<u>Dynamically-Tunable EBG Structure Demonstrator: Final Report</u> <u>Grant No. FA2386-10-1-4040 AOARD 10404</u>

Principal Investigator: Dr. Michael Heimlich Program Manager: Dr. Gregg Jessen

September 2011

Report Documentation Page		Form Approved OMB No. 0704-0188
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1. REPORT DATE	2. REPORT TYPE	3. DATES COVERED
05 OCT 2011	Final	22-06-2010 to 21-06-2011
4. TITLE AND SUBTITLE		5a. CONTRACT NUMBER
Electrically Tunable EBG Structure Demonstrator for IC-, Thick- or		FA23861014040
Thin-film Processing		5b. GRANT NUMBER
		5c. PROGRAM ELEMENT NUMBER
6. AUTHOR(S) Michael Heimlich		5d. PROJECT NUMBER
		5e. TASK NUMBER
		5f. WORK UNIT NUMBER
7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES) Macquarie University, Level 2, ,Building E6A,Sydney 2109,AU,2109		8. PERFORMING ORGANIZATION REPORT NUMBER N/A
9. SPONSORING/MONITORING AGENCY NAME(S) AND ADDRESS(ES) AOARD, UNIT 45002, APO, AP, 96338-5002		10. SPONSOR/MONITOR'S ACRONYM(S) AOARD
		11. SPONSOR/MONITOR'S REPORT NUMBER(S) AOARD-104040
12. DISTRIBUTION/AVAILABILITY STATEMENT Approved for public release; distribution unlimited		
13. SUPPLEMENTARY NOTES		
Electromagnetic Bandgap (EBG) structures exhibit large continuous regions as a function of frequency over which they will not allow a signal to propagate. A subclass of bandstop filters (BSF), EBG structures ?stop? a signal from passing through by having signals not propagate in abeyance of Maxwell?s Equations. Typically, EBG performance is achieved by modulating the geometric properties of an electromagnetic-guided or radiating structure so as to create a periodicity which induces the EBG and as such is not tuneable if implemented as integrated circuits (IC) or printed circuit boards (PCB). This work implements dynamic tuning by using RF/microwave switches to move the effective ground plane of a guided structure.		
15. SUBJECT TERMS meta materials, Radio Frequency Transmission Lines		

16. SECURITY CLASSIFICATION OF:

b. ABSTRACT

unclassified

a. REPORT

unclassified

17. LIMITATION OF ABSTRACT

Same as

Report (SAR)

c. THIS PAGE

unclassified

18. NUMBER

OF PAGES

8

19a. NAME OF

RESPONSIBLE PERSON

Introduction

Electromagnetic Bandgap (EBG) structures exhibit large continuous regions as a function of frequency over which they will not allow a signal to propagate. A subclass of bandstop filters (BSF), EBG structures "stop" a signal from passing through by having signals not propagate (vs. some other means of signal rejection, like reflection) in abeyance of Maxwell's Equations. Typically, EBG performance is achieved by modulating the geometric properties of an electromagnetic-guided or radiating structure so as to create a periodicity which induces the EBG and as such is not tuneable [1] if implemented as integrated circuits (IC) or printed circuit boards (PCB). This work implements dynamic tuning by using RF/microwave switches to move the effective ground plane of a guided structure. The aim was to create a PCB demonstrator based on the prior theoretical study on IC [2].

Detailed Project Objective

According to [2], the structure needs to have several key features (as shown in Figure 1):

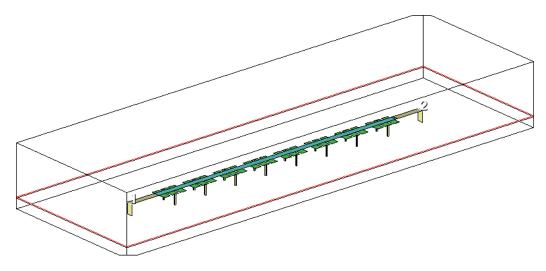


Figure 1 – Theoretical EBG structure for IC

- 1. A thick, low-loss dielectric substrate with a ground plane on the back. Bottom-most layer shown in box edges in Figure 1.
- 2. A top-layer metal conductor which, when placed on the top of item 1, implements a high-quality microstrip transmission line. Blue line in Figure 1.
- 3. A very thin, low-loss dielectric layer inserted between items 1 and 2. Middle (reddish) layer shown in box edges in Figure 1.
- 4. Periodic metal patches transverse to item 2 and on the bottom side of item 3(i.e. between the items 1 and 3). Green structures in Figure 1.
- 5. Conducting vias located beyond the ends of metal patches in item 4 which connect to the ground plane of item 1 through a selectable electronic switch capable of passing RF/microwave signals at some lower frequency switching rate; the switching speed is unimportant for this Demonstrator. Gold vertical rectangles in Figure 1.
- 6. Switches connecting the vias, item 5, to the patches, item 4. Not shown in Figure 1.

This structure, fabricated on a typical GaAs IC process was theoretically shown to have an EBG in the 60-150GHz range depending on the pattern of patches grounded using the switches.

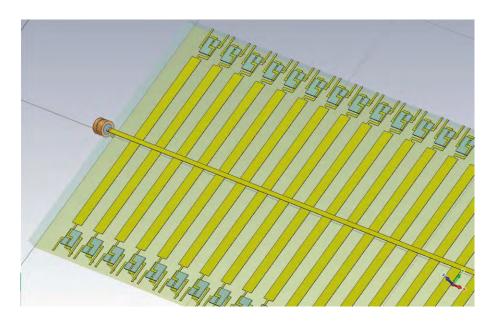


Figure 2 – initial design of Demonstrator

The objective of this project was to prototype the GaAs IC EBG design using printed circuit board (PCB) technology. The proposed project approach (Figure 2) was to use an alumina substrate with gold metallization for the thick layer, ground plane, and patches. A thin polyimide was to be applied using a spin-on technique with gold patterned on top of the polyimide for the transmission lines. Packaged microwave FET switches where to be placed on top, and using vias, connect the patches to the ground plane with control lines to turn the switches off and on running to the side edges of the PCB. SMA connectors placed at the ends of the microstrip transmission line would function as the signal input/output. A twenty-four patch design was chosen as a good trade-off between switching patterns and cost/complexity of manufacturing.

Results

Initial discussions with the cleanroom personnel at Macquarie deemed that the polyimide processing and metal patterning (of patches and microstrip line) could be done in our cleanroom facility. Vias in the polyimide could also be done. No capability for vias in alumina could be supported at Macquarie at the diameters necessary for the compact size of the structure. Investigation of external manufacturing capability yielded several potential fabricators for the vias but they could not be done with certainty prior to applying the polyimide and subsequent alignment of a polyimide vias with the alumina via was also an issue given the dimensions. The original structure as it was intended on IC was therefore abandoned.

A redesign of the structure was undertaken which required that the polyimide be etched back from the vias so that it was only within the area where the patch interacted electrically with the microstrip line. Electromagnetic (EM) simulation showed that this would exhibit the EBG effects as intended. This structure was not manufacturable at Macquarie and required expensive selective etching of the polyimide which had the potential of leaving chemical residues on the electrical pads for the switches, which would have severally impacted the yield of connecting 48 switches for the 24 patches. The cost/yield issues made this design unacceptable.

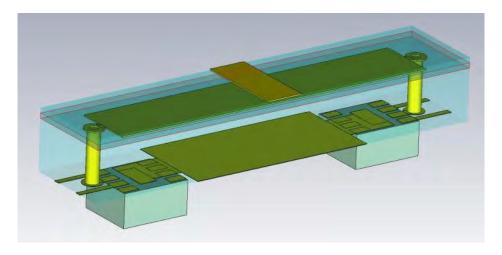


Figure 3 – Conceptual design used for fabrication of Demonstrator

A second redesign, Figure 3, moved the switches from the front to the back (adjacent to the ground plane). This had the drawback that the "patch" now included a via on each of its ends even when the switches controlling that patch were turned "off". However, this design greatly simplified manufacturing and had the added benefit that the dense control and bias lines for the switches (not shown in Figure 1) were on the back and isolated from the microstrip transmission line structure. This design was sent for PCB manufacturing and then for assembly of the FET switches. The final assembly of SMA connectors and electrical connector for the switch power and control at Macquarie (top-side in Figure 4).

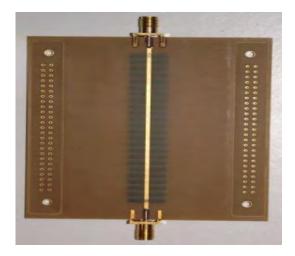


Figure 4 – Fabricated Demonstrator with SMA connectors, top-side. Switches not installed so as to test without switch-induced impairments to performance

A subset of PCBs were not sent for FET switch assembly and instead were used to evaluate the PCB itself, in the absence of switches, by soldering switches in a desired pattern in accordance with simulations. Reported results [3], Figure 5, showed EBG behaviour as predicted with EM simulation and in accordance with that expected from the original, theoretical work.

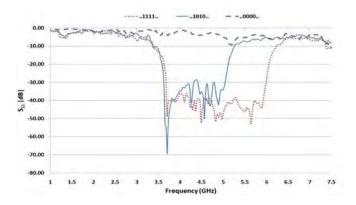


Figure 5 – EBG Demonstrator PCB with hard-wired patch configurations "...1111...", "...1010..." and "...0000.." [3]

The FET switches chosen for the Demonstrator were the MASW 007921 SPDT switch by M/A-COM Technology Solutions. A separate PCB test-structure was developed for the switch to evaluate its properties in a configuration similar to that with the EBG demonstrator. Reported results [4], seen in Figure 6, showed that the switch provided adequate insertion loss and isolation for the EBG demonstrator. The net effect of these results is that the FET device shifts the EBG of the structure up in frequency from the ideal case simulated with the EM solver.

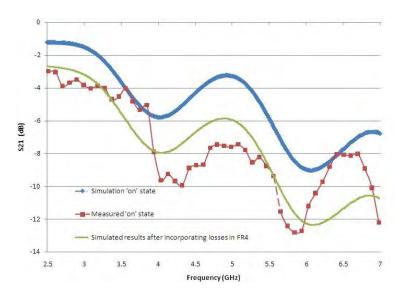


Figure 6 – Measured vs. Simulated on-state for FET switch in EBG Demonstrator configuration on special evaluation board.

The full-up Demonstrator (Figure 7) board was tested (Figure 8) over several different switch patterns. Results shown in Figure 9 are being prepared for publication [5] and are continuing to be analysed. An issue arising from the final manufacturing configuration is the coupling of the signal to the control lines and their role, given the finite insertion loss and isolation of the FET switches to the deep resonances seen in Figure 7. We are lead to this early conclusion as the EM analyses tend to be overly optimistic and these measured results exceed even them in terms of roll-off and rejection ratio relative to the "…0000…" through signal.

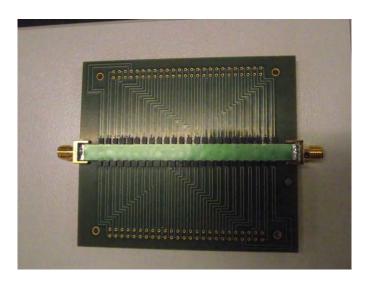


Figure 7 – Fabricated EBG Demonstrator with mounted switches

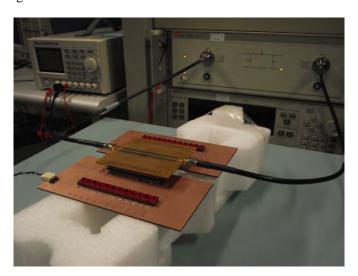


Figure 8 – Testing of EBG Demonstrator

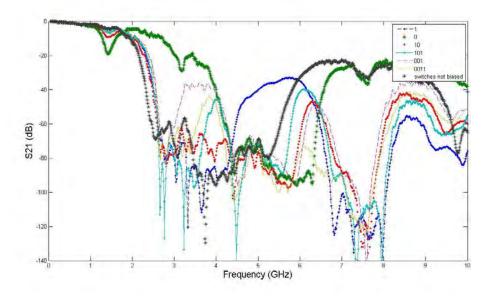


Figure 9 – Measured results of the EBG Demonstrator for several periodic configurations of the FET switches.

Work continues to analyze these results. Currently, a circuit model has been developed to provide a means for synthesizing patch size, width, spacing, and periodicity to achieve desired stopbands. This work is complicated by the fact that the propagation mode changes from quasi-TEM to leaky- or evanescent mode and then to higher order mode as the frequency goes from below, through, and above, the stopband, respectively. Additional methods of modelling, including rational-approximation and pole-zero, are being explored. Finally, this work has provided substantial validation of the overall theory that an IC implementation will be fabricated.

Conclusion

An EBG Demonstrator was successfully fabricated and tested using the initial, theoretical work on GaAs IC technology. For manufacturing cost and yield, an altered design was chosen. This design exhibits EBG performance very close to that predicted in terms of bandwidth as compared to EM analysis. The performance in terms of rejection ratio and roll-off is much better than anticipated. The reason for this behaviour is not clearly understood but is an area of on-going investigation.

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- [5] Publication in preparation.